# Power Reduction In Logic Circuits Using Power Gating For Deep Sub-Micron CMOS VLSI

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***Abstract***: Technology scaling leads to subthreshold leakages in deep submicron regime. There is a need for effective leakage reduction techniques to minimize leakage currents. This paper presents basic gates circuits and a full adder circuit with low power consumption. This crucial leakage reductions are achieved by turning off the logic cells from ground and supply rails by power gating technique. Power gating technique reduces static power consumption but it increases the delay of the logic cells badly in deep submicron CMOS circuits and the performance is besmirched to a great extent. In order to enhance performance additional transistors are added in the circuit which reduces both dynamic and leakage consumption enormously. Simulations are done with 45nm CMOS technology in Cadence Virtuoso. Circuits are working in 0.5V supply voltage. It reduces the static power without much affecting dynamic power consumption compared to those of equivalents. For the 10T full adder, the proposed design accomplish percent reduction in dynamic power consumption and percent reduction in static power consumption. The proposed designs are apt for low power and highly efficient adders.

Keywords: Power gating, retention, transistor stacking.

## I. Introduction

Electronic devices such as laptop, cell phone, digital camera etc. are part of our day today life. Its battery life span is of great importance. When the mobile phone is operating in talk mode, some components of the mobile phone are turned off, but this doesn't stop the battery from getting depleted. This is because circuits which are de-activated by turning off certain component parts still have leakage currents flowing through them. It decreases the battery life over relatively long standby time although the magnitude of leakage current is less than the normal operating current. The normal operating current reduces the battery life over relatively short talk time. Thus low power circuits for different applications are of great interest.

Power dissipation in CMOS circuits [1] comes from two components. Dynamic dissipation may be due to charging and discharging of load capacitances as gates switch, or “short-circuit” current while both PMOS and NMOS stacks are partially ON, whereas Static dissipation may be due to Sub-threshold leakage through OFF transistors, Gate leakage through gate dielectric, Junction leakage from source/drain diffusions and Contention current in ratioed circuits. Power can also be considered in active, standby, and sleep modes. Active power is the power consumed while the chip is in the working condition. It is usually dominated by switching. Standby power is the power consumed while the chip is in idle condition. In sleep

mode, the supplies to unneeded circuits are turned off to eliminate leakage [2]. This drastically reduces the sleep power required, but the chip requires time and energy to wake up so sleeping is only viable if the chip will idle for long enough. There are many proposed technique for power and energy reduction. Voltage supply (Vdd) scaling is considered one of the most effective elements in the process of reducing power dissipation in CMOS circuits. In order to maintain the required current drive, Threshold Voltage (Vth) has also be reduced. Reducing threshold voltage Vth results in an exponential increase in leakage power. The ratio Vdd /Vth tend to decrease with technology scaling to keep the leakage power under control. Another technique is power gating. In this, the power supply and the ground line are separated from the circuit block while the chip is in sleep mode.

In this paper, we synthesized NOT, NAND and NOR gates and proposed novel techniques to minimize power and to improve the performance of these gates in nanoscale technology [3]. Also, 1-bit 10 T full adder has been realized with power gating for the leakage power reduction in 45nm technology [4]. The rest of the paper is organized as follows. Section II describes the related work. Section III shows the design considerations and section IV presents the proposed design. Section V describes the implementation and simulation together with the simulation of a 1bit 10 T full adder. Finally, the conclusions are presented in section VI.

## II. Related Work

Ankita Nagar [5] proposed the reduction of power dissipation in basic gates using transistor stacking. It is found that when the number of low input increases in case of NAND gate the power dissipation decreases and for NOR gate power dissipation decreases with the increase in high input vector combination. Jatin Mistry, James Myers and Basher M [6] presents a technique called sub clock power gating. Amit Bakshi [7] gives an idea on reducing subthreshold leakage power consumption and ground bounce noise during the sleep to active mode transition. Shota Ishihara, Masanori Hariyama [8] gives the classification of power gating technique as fine grain power gating and coarse grain power gating. In coarse grain power gating a single sleep transistor is shared among all the components whereas in finegrain power gating each component will have sleep transistors. In order to reduce subthreshold leakage in sleep mode Seta et al applied reverse body bias [9] for deep submicron circuits. T Kuroda et al proposed variable threshold CMOS [10]using TWIN well or triple well technology. An extra circuitry to apply bias to the footer was proposed by Kawaguchi et al [11] and this technique is called super cut off CMOS power gating. Large cores power deduction is possible through multi-mode power switches.It is proposed by Zhaobo Zhang et al by using three transistors attached to footers to the main core to operate in four modes such as active mode, snore mode, dream mode and sleep mode. In this paper we proposed a design to reduce the power consumption using power gating with reverse body bias and extra devices to improve performance.

## III. Design Considerations

Supply voltage scaling is an important step in the technology scaling process. Supply voltage scaling helps in maintaining the power density of an integrated circuit below a

limit dictated by available cost effective cooling techniques and it also guarantees the long term reliability of the devices fabricated in a scaled semiconductor technology. In current CMOS technologies, dynamic power dissipation due to switching is the main component of the total energy consumption of an integrated circuit. The dynamic switching energy is proportional to the square of the supply voltage in a full voltage swing CMOS circuit. Moreover the leakage and short circuit energy components also depend super linearly on the supply voltage. Reducing the supply voltage, therefore, is an effective way to lower the power dissipation.

Power gating is one of the technique to reduce the leakage power. Power gating uses PMOS or NMOS as sleep transistors that are having low leakages. Power gating consists on switching off the power supply from blocks that are in standby mode and switching the power back on when their functionality is required. In order to switch power off, high Vt transistors are used as switches and placed between the block power and ground pins and the rails. Header Switch which is a PMOS transistor is placed between the power pins and the power rails. Footer switch which is a NMOS transistor placed in between the ground pins and ground rails. This way the controlled block, is no longer powered by the main power rails (always-on rails), but by a switched/virtual power rail. The control of the power switches is achieved through an enable or sleep signal. For a header switch, the enable signal takes the logic value 1 in order to switch power off. In the footer switch case, the opposite happens. As important as the power switches themselves is to distribute and deliver power in the best way possible across the whole design. The power network should be designed to minimize the voltage drop and to correctly power all blocks and standard cells in the design. Additionally, a state retention strategy can be implemented. Depending on the application, it can be necessary to save the state of the block. This way, when power is switched back on, the block can return to the exact same functioning state [14]. This is achieved by using state retention transistors. It may be also important to isolate the powered-off block output signals. These signals, if floating, can induce a crow-bar current in an adjacent block, to which represent input signals. Sub-threshold leakage current that is flowing through a stack of series-connected transistors decreases when more than one transistor in the stack is turned off. This effect is known as stacking effect. It is also known as self-reverse bias. Leakage currents in NMOS or PMOS transistors depend exponentially on the voltage at the four terminals of transistors [15]. The gate voltage Vg is “0” and this will increase source voltage Vs of NMOS transistor. This reduces sub-threshold leakage current exponentially. In our design we consider transistor stacking, retention transistor and novel hybrid technique to reduce the power consumption.

## IV. Proposed Work

NOT Gate

Novel hybrid NOT gate

The design of a hybrid NOT gate is shown in fig 1.The circuit contain an inverter design with sleep transistors. In the static mode, the sleep transistors P0 and N1 are off. Therefore the logic circuit is isolated from supply and ground rails. So the static power is almost low. In the dynamic mode the sleep transistors are on and when the input is zero, PMOS P3 will

be ON and the little leakage current in the NMOS N0 is fedback to the input through the PMOS P3 and thereby the dynamic power is reduced. When the input is high, PMOS P3 will be OFF and the NMOS N0 would be ON and it is connected to ground through high threshold voltage transistor N1. This low voltage threshold PMOS P3 added to the input of the inverter increases the throughput. The source and gate of this PMOS is shorted. Its drain is connected to the ground and also fed to the virtual ground. This low threshold voltage transistor is used to minimize the standby leakage.

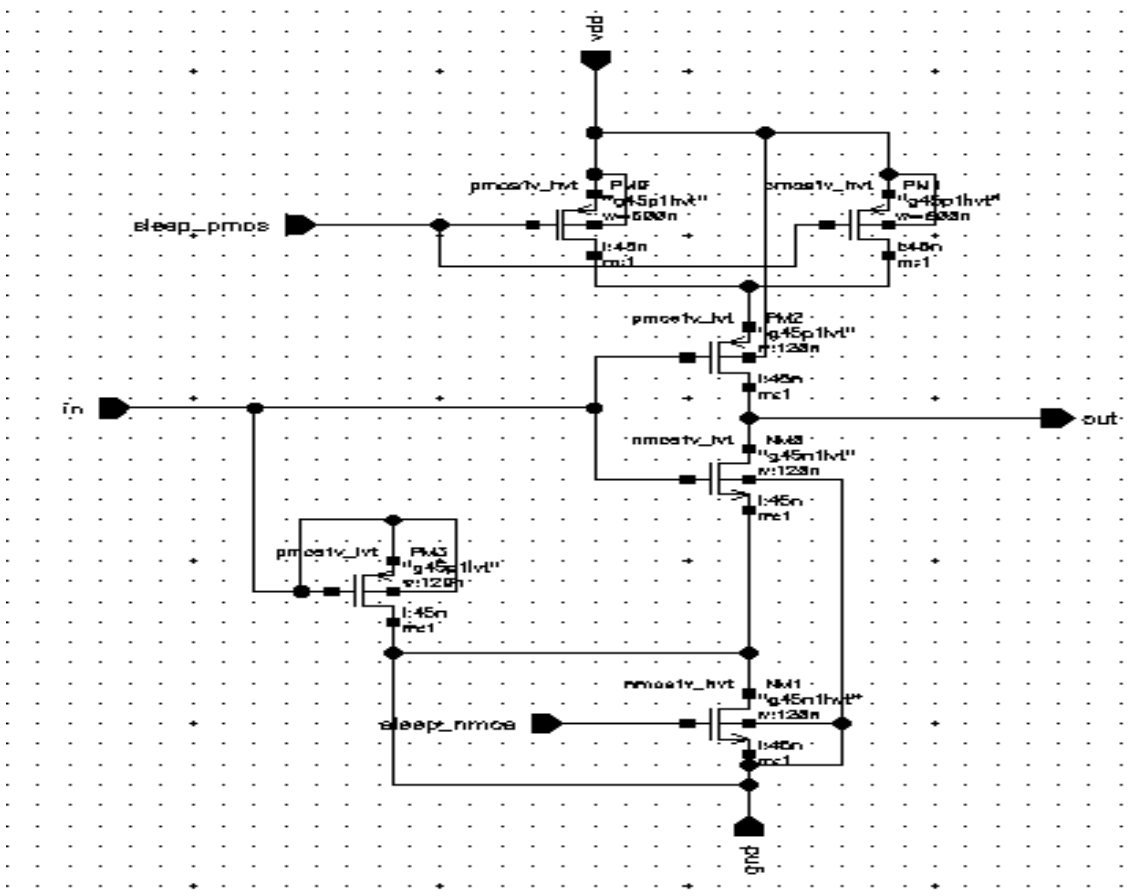


Fig.1 Novel Hybrid NOT gate

Novel Hybrid NOT gate with transistor stacking

In this design transistor stacking is employed. Here instead of one transistor in the logic circuit, two PMOS/NMOS transistors (P2, P3 and N0, N1) are placed one over the other. It will not affect the total width or length of the transistors. But the standby power is reduced further because leakage current through a stack of two off transistors will be less than that of a single off transistor. The dynamic power consumed will be more as extra transistors are used in this technique. When such series connected NMOS transistors N0 and N1 are turned off, the internal node makes the gate to source voltage of upper transistor N0 to be negative. Hence the subthreshold leakage current is reduced. Care should be taken such that addition of extra transistors should not impact adversely the performance of the logic circuit. In order to improve

the performance of a static CMOS inverter a low threshold voltage transistor PMOS P4 is connected. Also by applying a body bias using an extra circuitry standby leakage can be further suppressed.

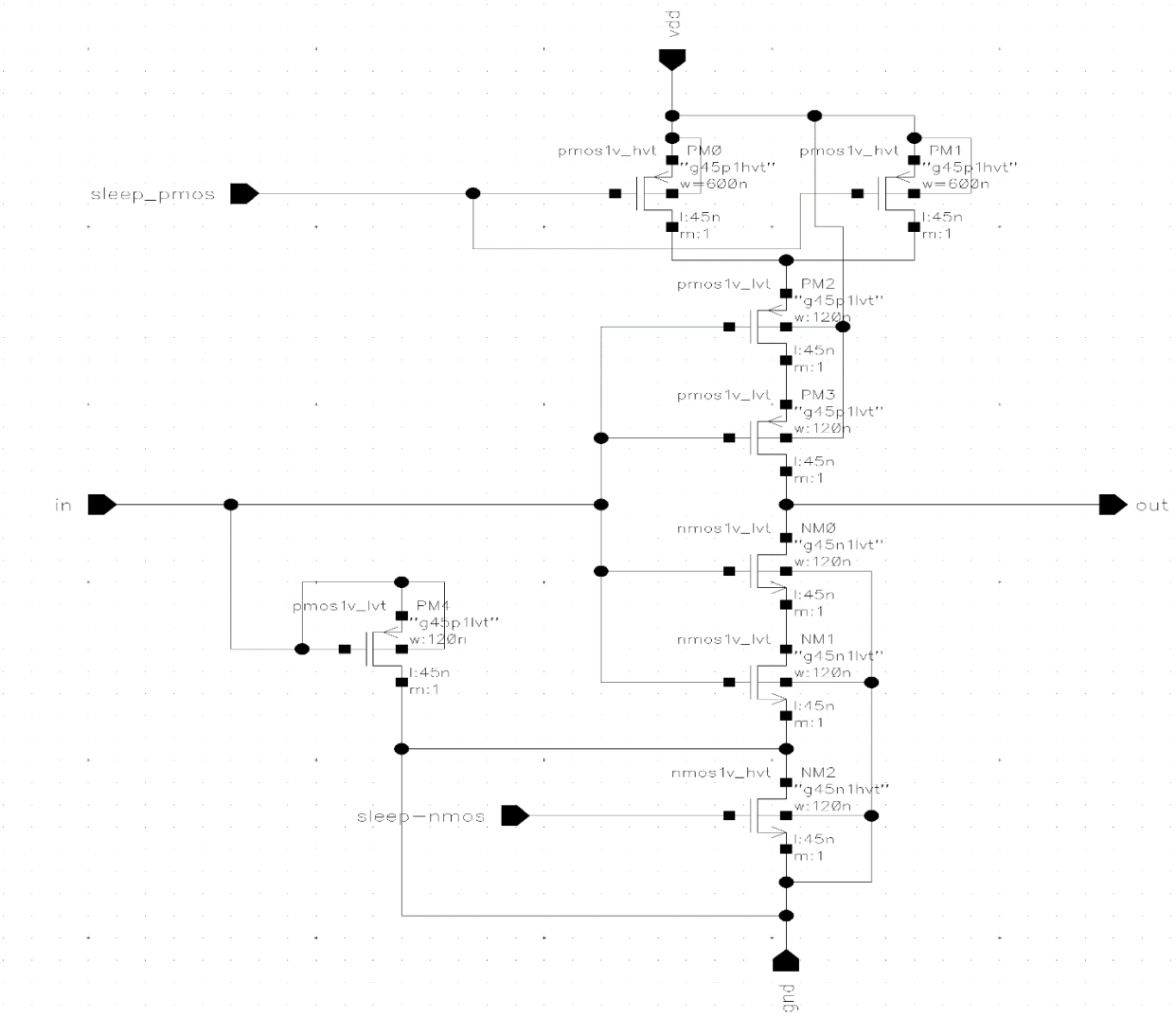


Fig 2. Novel Hybrid NOT gate with transistor stacking.

Novel Hybrid NOT gate with retention transistor

Here the circuit is designed with retention transistors is shown in fig 3. Here symmetric virtual rail clamping technique is employed. This technique work by reducing the virtual supply to less than Vth rather than shutting down completely as in the case of conventional power gating. Symmetrical Virtual rail clamping is used to achieve reduced voltage. For this a pair of NMOS and PMOS transistors are used at the head and foot of the power gated logic. A high threshold NMOS transistor N2 is connected parallel to high threshold PMOS transistors P0 and P1 in the pullup network and also a high threshold PMOS transistor P4 is connected parallel to high threshold NMOS transistor N1 in the pulldown network.

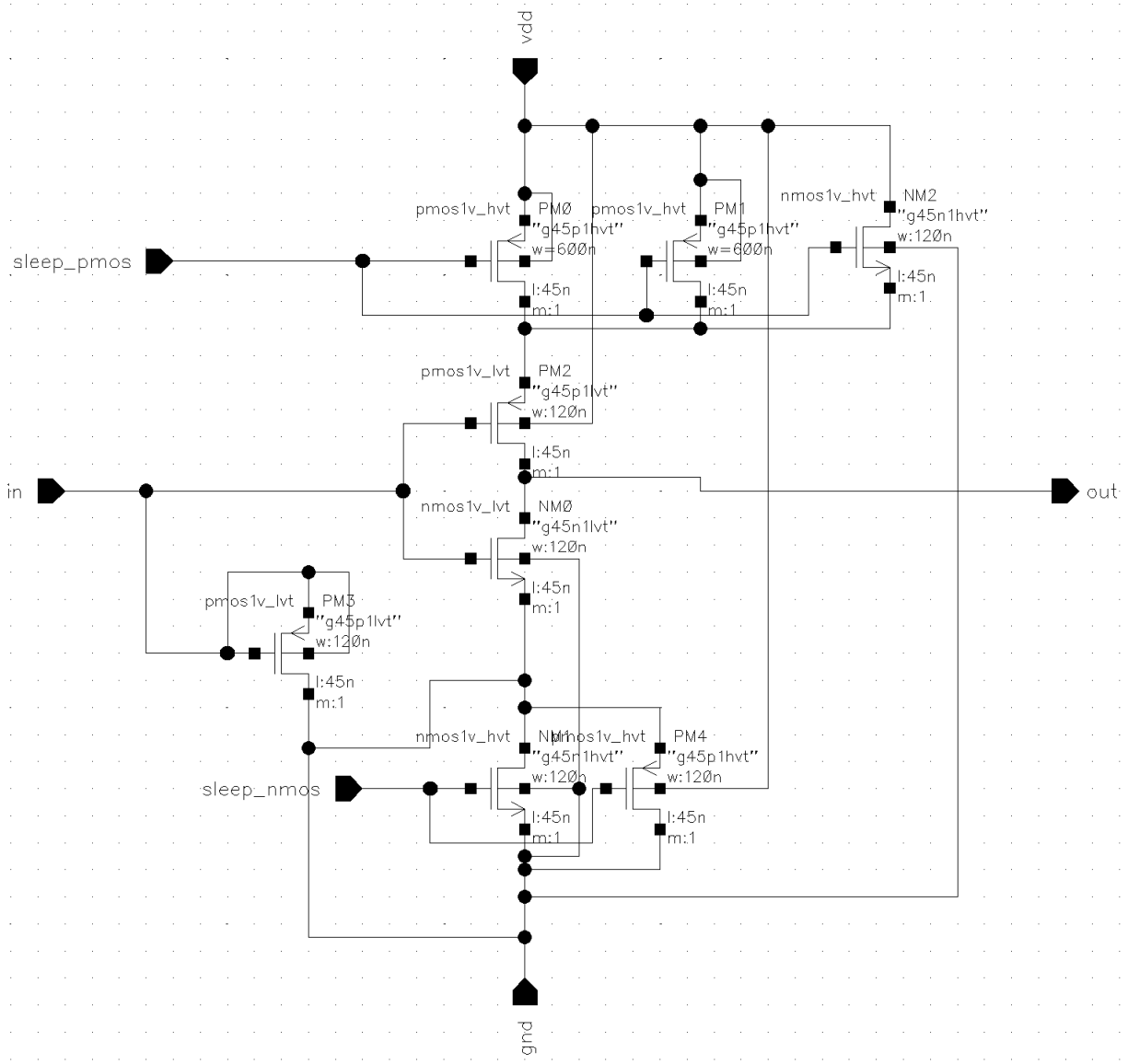


Fig 3.Novel Hybrid NOT gate with retention transistor

In the static mode when sleeppmos and retention transistors are given logic high, virtual supply rail is clamped to $V_{dd}$ -$V_{thn}$ and virtual ground rail is clamped to $V_{dd}$+$V_{thp}$, where $V_{thn}$ and $V_{thp}$ are the threshold voltages of the NMOS N2 and PMOS P4 transistors. This results in enormous reduction in voltage across power gated logic due to the following reasons. The first reason is that the charge stored in the supply rails is recycled back to charge the virtual ground rail in sleep mode through the PMOS P4.The second reason is that by connecting the PMOS body and NMOS body in the power gated circuit to the actual supplies achieves a new threshold voltage due to reverse body bias on all the transistors in the logic circuit which reduces leakage further. The third reason is that virtual rail clamping helps gates to keep its correct output for minimum supply voltages. Also in the static mode, when the input is low, PMOS P3 would be ON and thereby voltage in the virtual ground is fed back to the input and thereby static power is reduced.

On the other hand, when the input is high, PMOS P3 would be OFF and voltage in the virtual ground could not be fedback to the input. Hence static power reduction is more only when the input is low. In the dynamic mode when sleeppmos (P0, P1) and retention (N2) are given logic low, dynamic power is reduced more compared to the previous circuits as fewer number of transistors are ON in this technique.

NAND Gate

Novel Hybrid NAND gate

In the dynamic mode, when both inputs are high, both the NMOS, N4 and N3 in the pull down network are ON and the high threshold PMOS transistor P2 is OFF and the output goes low as all the transistors in the pullup network are OFF and current from the pull down network flows back to the input through this transistor P2 thereby reducing the dynamic power consumption. Here the PMOS transistor P2 whose gate and source is tied together and anyone of the inputs is given to the gate/source and the drain is connected to both ground and virtual ground as shown in fig 4.This extra HVT transistor supports in the reduction of dynamic and standby power consumption to a large extend without degrading the circuit performance. The output of CMOS NAND gate is high when any one of the input is low. On the other hand, when both inputs are high, the output is low. When both inputs are low, the outputs goes high as both the PMOS transistors in the pull up network are ON and both the NMOS transistor in the pulldown network are OFF.A part of the current in the transistor N2 flows through high threshold PMOS P2 as it is ON and thereby reducing dynamic power consumption.

When the inputs IN1 and IN2 are High and low then high threshold PMOS transistor P2 is ON and the output goes High as the PMOS transistor P3 is ON and the current in the NMOS transistor N4 flows back to the input through the high threshold PMOS P2 thereby reducing dynamic power. When the inputs are low and high then the high threshold transistor P2 is OFF and the output goes High as the PMOS transistor P4 is on and the current flowing in the NMOS transistor N1 drains to the ground through reverse body biasing. In the active mode, pmossleep and nmossleep are set Low and High respectively and the sleep transistors P0, P1 and N2 are turned on. As these sleep transistors ON resistances are small, the virtual supply rail more or less functions as the actual power rail. In the standby mode, power gating technique reduces the leakage power by using pmossleep and nmossleep. In the standby mode. pmossleep and nmossleep are set High and Low respectively and the sleep transistors are turned OFF, detaching the NAND gate circuit from the power supply and ground lines. This scheme reduces leakage power to a large extent and also the dynamic power consumption of the circuit is reduced but it increases area and delay of the circuit. Since the NMOS ON-resistance is smaller for the same width compared to PMOS, NMOS high threshold transistors are sized smaller compared to high threshold PMOS transistors.

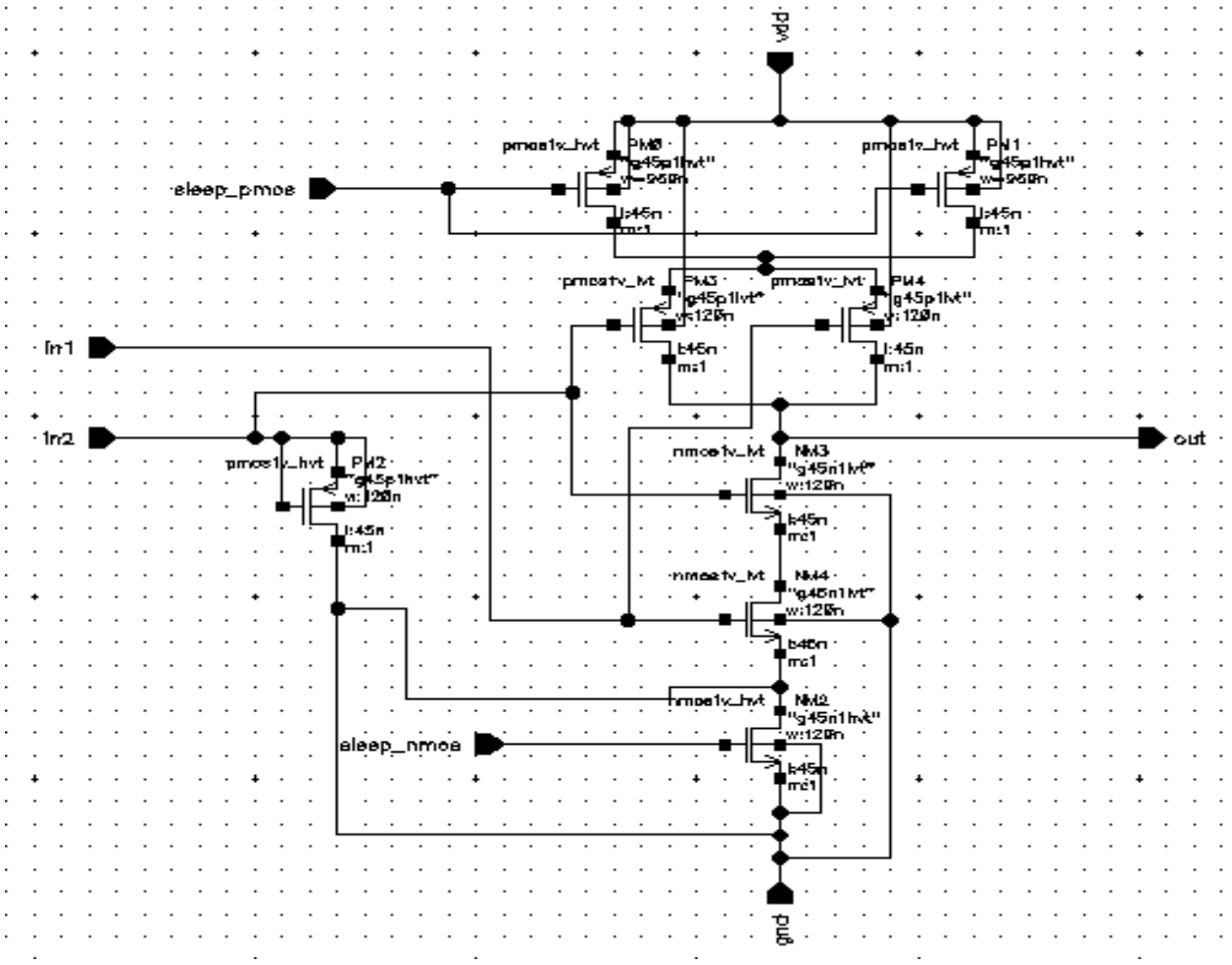


Fig 4.Novel Hybrid NAND gate.

Novel hybrid NAND gate with transistor stacking

One way of influencing the throughput of the static NAND circuit is by adding an extra device, a high threshold voltage PMOS P6. Here the PMOS transistor P6, whose gate and source is tied together and any one of the inputs is given to the gate/source and the drain is connected to both ground and virtual ground as shown in Fig. 5. This extra HVT transistor supports in the reduction of dynamic and standby power consumption to a large extent without degrading the circuit performance. The CMOS NAND gate output goes high when any one of the input is Low. Alternatively, when both inputs are High, the output is Low. Moreover reverse body bias and transistor stacking techniques are applied to reduce standby leakage power. In the active mode, pmossleep and nmossleep are set Low and High respectively and the sleep transistors P0, P1 and N4 are turned ON. As these sleep transistors ON resistances are small, the virtual supply rail more or less functions as the actual power rail. When both inputs are high the output is low as all the PMOS transistor in the pull up network are OFF and all the NMOS transistors (N0, N1, N2 and N3) in the pull down network are ON and the current flows to the

ground through NMOS transistor N4 and thereby reducing dynamic power consumption. Likewise when both the inputs are low all the NMOS transistor in the pull down network are ON and the current in the HVT transistor N4 flows through the HVT PMOS transistor P6 as it is ON and thereby reducing dynamic power consumption.

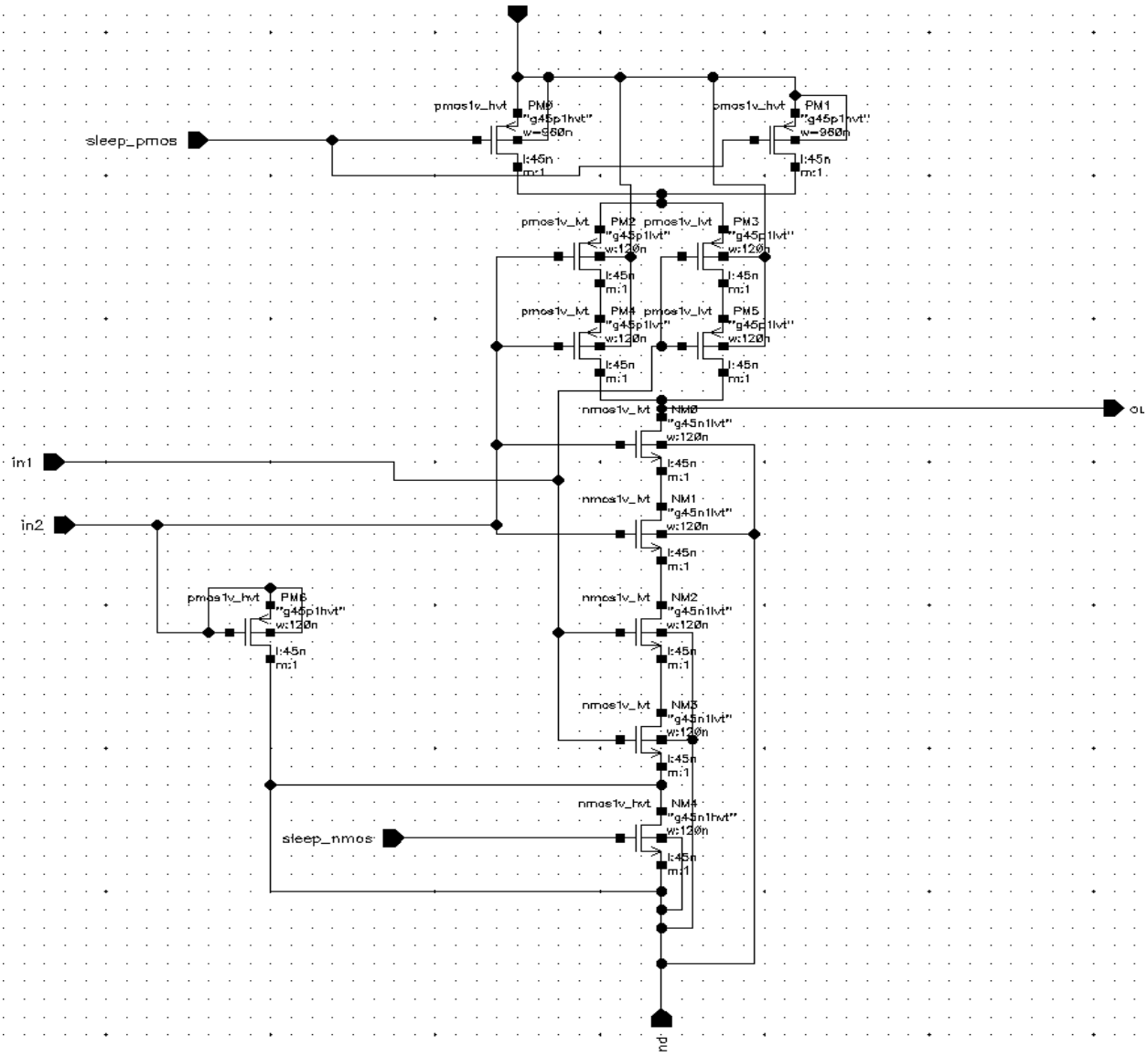


Fig 5.Novel Hybrid NAND gate with transistor stacking

When the IN1 and IN2 are high and low respectively, the output is high as PMOS transistors P2 andP4 are ON and HVT PMOS transistor P6 is ON and the current in the NMOS transistors (N2 and N3) flows back to the input through the PMOS P6 thereby reducing dynamic power. When the inputs IN1 and IN2 are low and high respectively, then the PMOS P6 is OFF and the output is high as the transistors P3 and P5 are ON and N2 and N3 are OFF and the leakage current flowing through the NMOS Transistor N0 and N1/ drains to the ground through reverse body

biasing. In case of standby mode power gating technique reduces the leakage power by using pmossleep and nmossleep.in the standby mode, pmossleep and nmossleep are set High and Low respectively and the sleep transistors are turned off, detaching the NAND gate circuit from the power supply and ground lines. This scheme reduces leakage power to a large extent and also the dynamic power consumption of the circuit is also reduced but it increases area and delay of the circuit.

HVT NMOS transistors are sized smaller compared to HVT PMOS transistors. Using transistor stacking in the NAND gate circuit increases the resistance and results in maximum reduction of sub threshold leakage current flowing through a stack of series connected transistors when more than one transistor is turned off in the stack. Here due to stacking effect, the subthreshold leakage current through a logic gate dependent on the states of the primary inputs. But the dynamic power of this circuit is increased as more number of transistors is utilized in this circuit.

Novel hybrid NAND gate with retention transistor

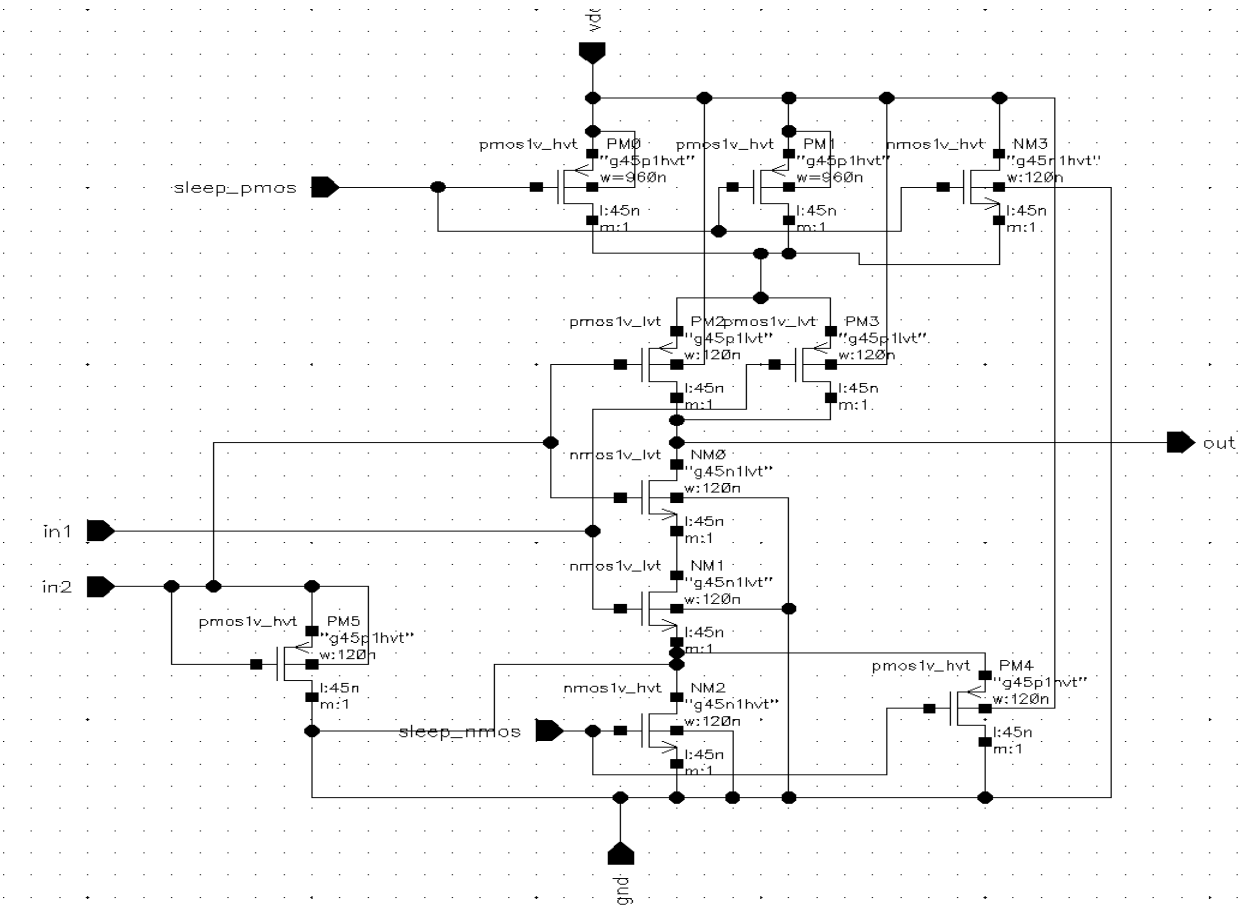


Fig 6.Novel Hybrid NAND gate with retention transistor

Here Virtual rail clamping has been introduced as a way to maintain a voltage across the power gated logic to retain register state. This technique reduces the recharge, glitching and wake up cost associated with power gating, as valid logic outputs are maintained. In general virtual rail clamping ensures a single voltage drop reduction across the power gated logic. But in order to increase the leakage power savings of power gated logic, symmetric virtual rail clamping is used to reduce the clamped voltage by two threshold voltages. Using this technique static power consumption is reduced to a large extent. Also symmetric virtual rail clamping causes the NAND gate to hold its output for very low supply voltages also. Moreover the dynamic power consumption is also deceased as the number of transistors used here is less compared to the previous circuit. Fig 6 shows the circuit of NAND gate with data retention transistors.

NOR Gate

Novel Hybrid NOR gate

In the dynamic mode, when both inputs are High, these two high threshold voltage NMOS transistors N0 and N1 are ON and also the two NMOS N2 and N3 in the logic circuit are ON. As the output is pulled to zero, the current through these two transistors N2 and N3 are fed back to the input through these HVT NMOS transistors N0 and N1 and thereby reducing the dynamic power consumption. When input In1 is Low, the transistor P2, connected next to Vvdd in the logic circuit is ON and the same input is fed to the high threshold transistor P4 whose gate and drain are shorted. This switches ON the high threshold voltage PMOS P4 whose source is connected to Vvdd trying to pull up the output High. If the input In2 is high, then the PMOS P3 is OFF and thereby pulling the output to Low. On the other hand, if the input In2 is also Low, then the PMOS P3 is ON and the NMOS N2 and N3 are OFF and thereby the output is pushed high. When the input In1 is High andIn2 is low, then the PMOS P2 is OFF and the PMOS P3 is ON and the high threshold PMOS P4 is also OFF. Even though this PMOS P4 is ON, this transistor is no more connected to supply voltage as the PMOS P3 is OFF and hence the output goes Low. Fig 7 shows the circuit of novel hybrid nor gate.

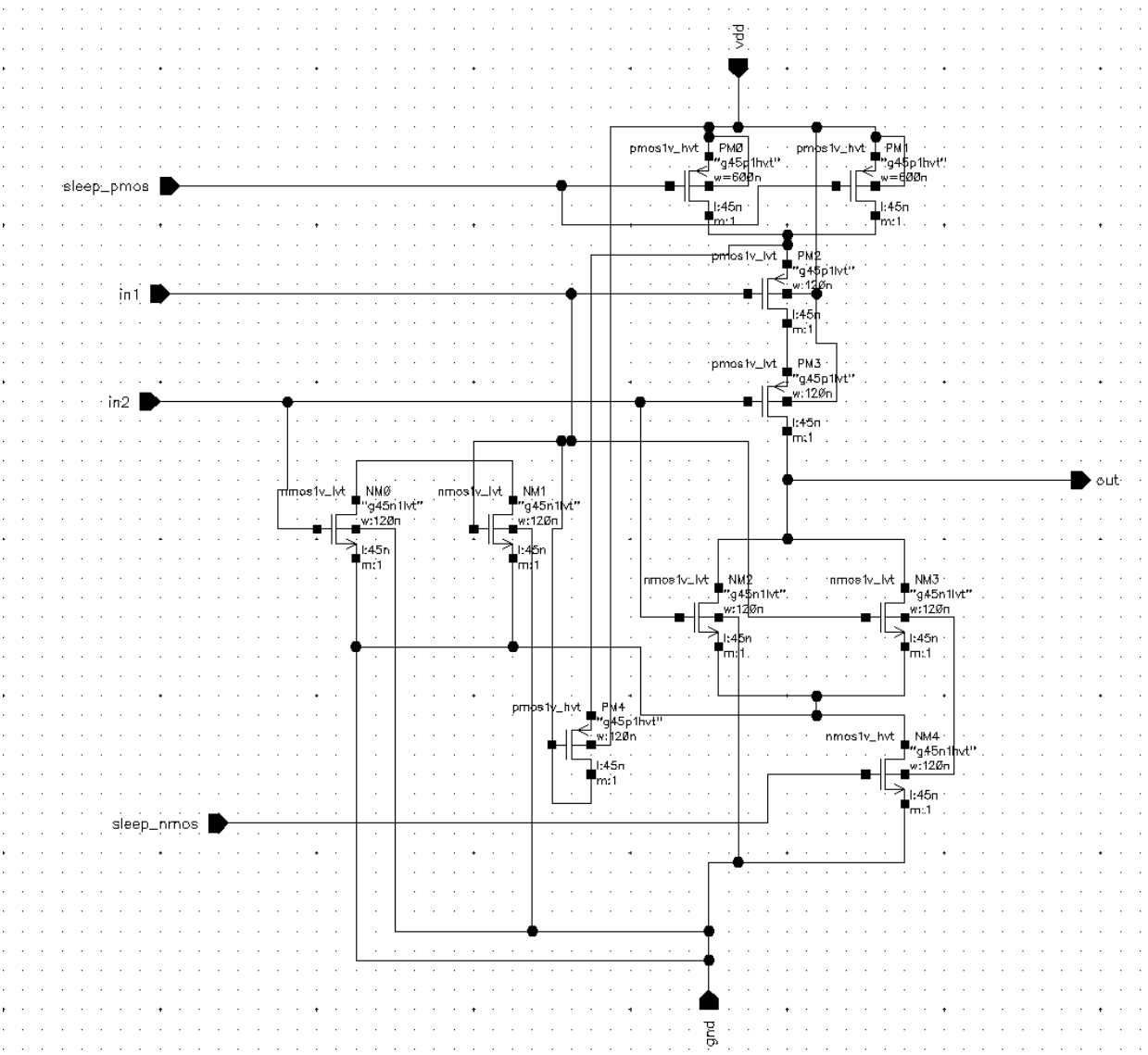


Fig 7.Novel Hybrid NOR gate.

Novel hybrid NOR gate with transistor stacking

In this circuit two high threshold voltage NMOS transistors N0 and N1 are connected as shown in fig 8.and their source are tied together to the virtual ground VGND and another high threshold voltage PMOS P6 is connected with gate and drain shorted and its source is connected to virtual supply Vdd. This technique employs transistor stacking. This technique helps in the maximum minimization of leakage power. In general the output of the NOR gate is low if any one of the input is High and the Output is high if both the inputs are low. In this transistor stacking technique, the resistance between the power supply and actual ground increases and thereby large percentage of the leakage power gets reduced. Addition of high threshold voltage transistors over the transistor stacking of logic circuit helps in the further

reduction of leakage power compared to simple power gating technique. Also supply voltage is reduced to 0.5V which helps to achieve definite reduction in active and standby power.

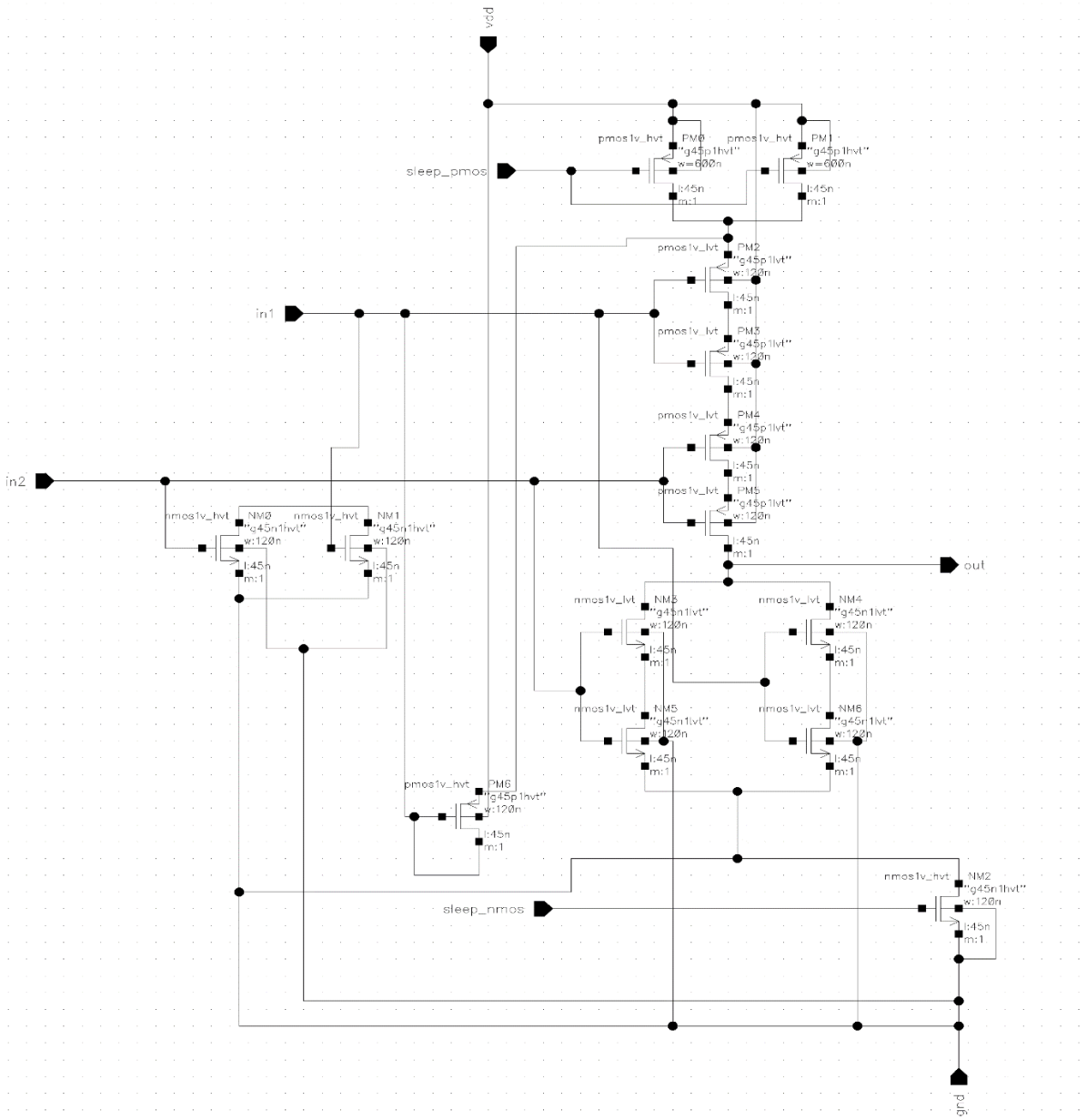


Fig 8.Novel Hybrid NOR gate with transistor stacking

In the dynamic mode, when both the inputs are high these two HVT NMOS N0 and N1 are ON and also all NMOS transistors in the logic circuit are also ON.As the output is pulled to zero, the current through these transistors N3, N5, N4 and N6 are feedback to the input through these HVT NMOS transistor N0 and N1 and thereby reducing dynamic power consumption. When the inputs IN1 is low, the transistors P2 and P3, connected next to Vdd in the logic circuit is on and also the same input is fed to HVT PMOS transistor P6.This switches on the HVT PMOS P6 whose source is connected to Vdd, trying to pull up the output high. If the input IN2 is high, then

the PMOS transistors P4 and P5 are off and thereby pulling the output LOW. On the other hand, if the other input IN2 is also low, then the PMOS transistors P4 and P5 are on and thereby the output is pushed high. When the input IN1 is high and IN2 is low then the PMOS P2 and P3 are off and high threshold voltage PMOS P6 is also off and the PMOS transistors P4 and P5 are on. Even though these PMOS transistors P5 and P6 are on, these transistors are no more connected to supply voltage as the PMOS P2 and P3 are off and hence the output is low.

Novel Hybrid NOR gate with retention transistors

In the second technique, retention transistors N5 and P5 are employed to preserve the output values. Using feedback connection in the circuit, in general preserves the output of the circuit. But here addition of HVT NMOS transistor N5 in parallel to HVT PMOS transistors and the addition of HVT PMOS transistor P5 in parallel to HVT NMOS transistor N4 help in retaining the output. This technique helps in reducing the leakage power to some extent and also the dynamic power of the circuit. In the static mode, when both the inputs IN1 and IN2 are high, the transistors P2 and P3 are off and hence no more attached to supply rail. Hence in these two cases, static power is greatly reduced. Moreover reverse body bias is employed in all the techniques to increase the threshold of the transistor in the standby state. Reverse body biasing is done by connecting the PMOS substrate to the supply rail and thereby increasing N well voltages of the PMOS. Hence the effective threshold of the PMOS transistor are increased which subsequently helps in the leakage current reduction in PMOS transistors. Similarly, by connecting the NMOS substrate to the ground rail increases the P-well voltages of the NMOS, which helps to raise the NMOS threshold and thereby leakage reduction occurs in the NMOS transistors. But a large voltage is required to achieve a mall rise in the threshold voltage. Hence this method is less effective.

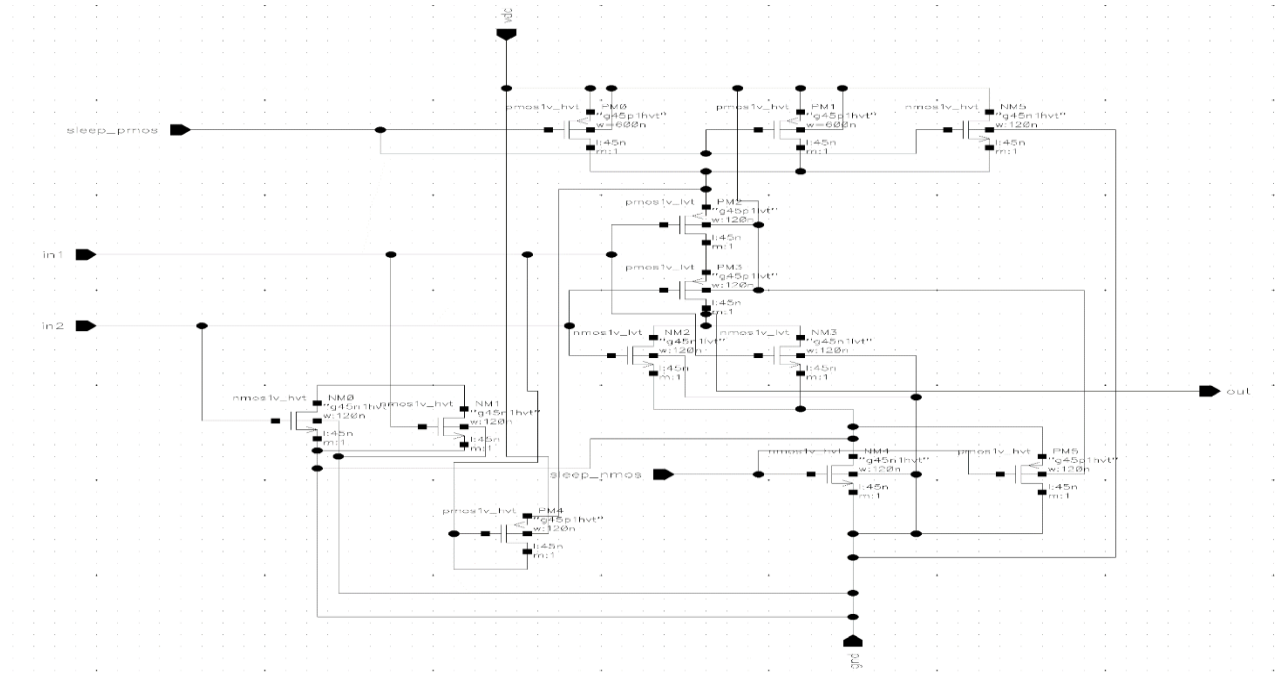


Fig 9.Novel Hybrid NOR gate with retention transistor.

For the proposed techniques, the width of the High Threshold Voltage transistor (HVT) and the list of high voltage transistors used in the circuit are tabulated in table I, II and III.

Table I
HVT TRANSISTORS AND WIDTH OF HVT TRANSISTORS UTILIZED IN NOT GATE

| Technique | HVT Transistors | Width of power gating PMOS transistors(nm) | Width of power gating NMOS transistor (nm) |
|---|---|---|---|
| Novel Technique | P0,P1,N1 | 600 | 120 |
| Novel Technique with transistor stacking | P0,P1,N2 | 600 | 120 |
| Novel Technique with retention transistor | P0,P1,P4,N1,N2 | P0,P1-600<br>P4-120 | 120 |

Table II
HVT TRANSISTORS AND WIDTH OF HVT TRANSISTORS UTILIZED IN NAND GATE

| Technique | HVT Transistors | Width of power gating PMOS transistors(nm) | Width of power gating NMOS transistor (nm) |
|---|---|---|---|
| Novel Technique | P0,P1,P2,N2 | P0,P1-960<br>P2-120 | 120 |
| Novel Technique with transistor stacking | P0,P1,P6,N4 | P0,P1-960<br>P6-120 | 120 |
| Novel Technique with retention transistor | P0,P1,P5,P4,N2,N3 | PI,P2-960<br>P5,P6-120 | 120 |

Table III
HVT TRANSISTORS AND WIDTH OF HVT TRANSISTORS UTILIZED IN NOR GATE

| Technique | HVT Transistors | Width of power gating PMOS transistors(nm) | Width of power gating NMOS transistor (nm) |
|---|---|---|---|
| Novel Technique | P0,P1,P4,N4 | P0,P1-600<br>P4-120 | 120 |
| Novel Technique with transistor stacking | P0,P1,P6,N0,N1,N2 | P0,P1-600<br>P6-120 | 120 |
| Novel Technique with retention transistor | P0,P1,P4,P5,N0,N1,N4,N5 | P0,P1-600<br>P4,P5-120 | 120 |

## V. SIMULATION RESULTS

We applied different techniques to reduce the dynamic and static power consumption of NOT, NOR and NAND gate. All the design are done and simulation is performed in Cadence design environment using 45 nm technology. The power dissipation is measured during active mode and standby mode of operation for all circuits. In the static mode, power gating PMOS transistor are constantly maintained at 0.5V and power gating NMOS transistor are connected to ground potential. In the active mode, power gating PMOS transistor are connected to ground and NMOS transistors are connected to 0.5V supply. The period and the pulse width of the input are set as 1.5ns and 750ps respectively. The rise time and fall time are set within 50ns for NOT gate and 82ns for NAND and NOR gate.

The static and dynamic power dissipation during all operating modes are measured by using CADENCE result browser and calculator. Table IV and V summarizes the simulated results of standard NOT gate with novel hybrid technique, transistor stacking technique and retention transistor technique. Figures 10 shows the simulated output waveform of hybrid NOT gate.

Table IV
DYNAMIC POWER CONSUMPTION OF NOT GATE

| INPUTS | Standard CMOS (nw) | Novel Hybrid technique (nw) | Novel Technique with transistor stacking (nw) | Novel Technique with retention transistor (nw) |
|---|---|---|---|---|
| 0 | 131.6 | 41.64 | 11.87 | 41.72 |
| 1 | 131.1 | 41.46 | 13.78 | 41.39 |

From the dynamic power consumption result obtained, we can clearly see that the dynamic power consumption is reduced compared to the standard CMOS NOT gate and the transistor stacking technique have the least power consumption.

Table V
STATIC POWER CONSUMPTION OF NOT GATE

| INPUTS | Standard CMOS (pw) | Novel Hybrid technique (pw) | Novel Technique with transistor stacking (pw) | Novel Technique with retention transistor (pw) |
|---|---|---|---|---|
| 0 | 4.14 | 13.71 | 2.389 | 11.87 |
| 1 | 3.94 | 2.69 | 13.68 | 13.78 |

From the above result we can see that the leakage power consumption is reduced with the novel techniques.

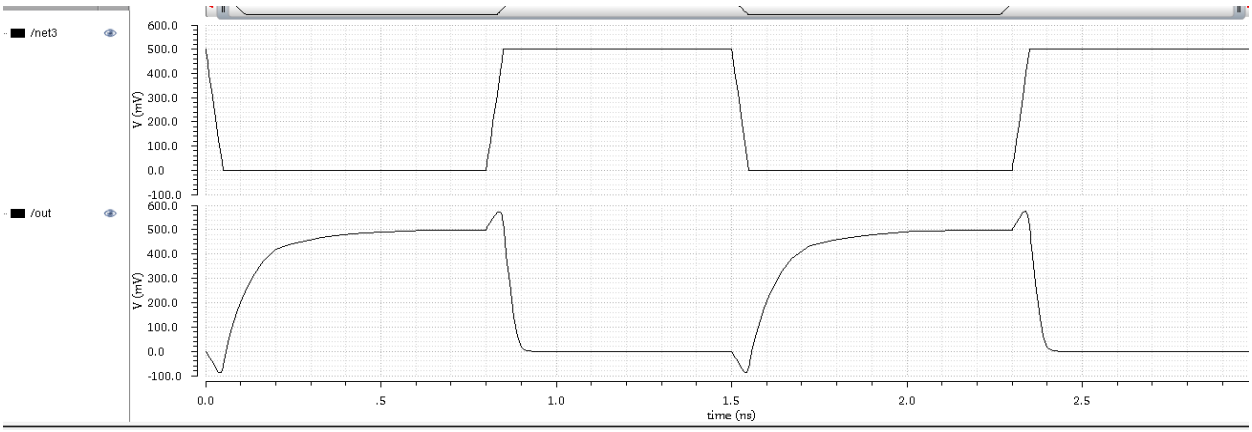


Fig 10.Novel Hybrid NOT gate

Delay of NOT gate with different techniques are given in table VI. Delay is less in retention transistor technique.

Table VI
Delay of NOT gate

| INPUT | Standard CMOS (ps) | Novel Hybrid Technique (ps) | Novel Technique with transistor stacking (ps) | Novel technique with retention transistor (ps) |
|---|---|---|---|---|
| 0 | 120 | 44 | 81 | 44.4 |
| 1 | 174 | 90 | 141 | 85 |

Table VI and VII summarizes the simulated results of standard NAND gate with novel hybrid technique, transistor stacking technique and retention transistor technique. Figures 11 shows the simulated output waveform of NAND gate with transistor stacking.

Table VI
DYNAMIC POWER CONSUMPTION OF NAND GATE

| INPUTS | Standard CMOS (nw) | Novel Hybrid technique (nw) | Novel Technique with transistor stacking (nw) | Novel Technique with retention transistor(nw) |
|---|---|---|---|---|
| 00 | 204 | 66.94 | 78.54 | 66.88 |
| 01 | 93.85 | 20.29 | 26.69 | 20.09 |
| 10 | 38.61 | 7.213 | 6.653 | 17.1 |
| 11 | 217 | 66.13 | 69.57 | 66.15 |

Table VII
STATIC POWER CONSUMPTION OF NAND GATE

| INPUTS | Standard CMOS (pw) | Novel Hybrid technique (pw) | Novel Technique with transistor stacking (pw) | Novel Technique with retention transistor(pw) |
|---|---|---|---|---|
| 00 | 1.44 | 2.951 | 1.621 | 4.486 |
| 01 | 4.14 | 4.423 | 3.443 | 12.37 |
| 10 | 3.83 | 3.922 | 2.909 | 11.78 |
| 11 | 7.89 | 1.499 | 1.495 | 1.622 |

Even in all these techniques, novel technique with transistor stacking consumes less static power. But the dynamic power consumption is less in the case of novel technique with hybrid NAND and retention transistors.

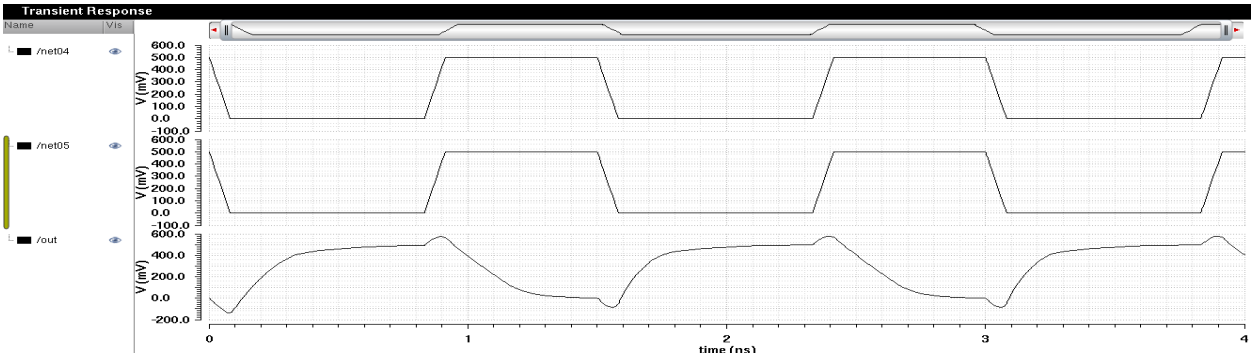


Fig 11 .Novel hybrid NAND gate with transistor stacking

Table VII
DELAY OF NAND GATE

| INPUT | Standard CMOS(ps) | Novel Hybrid Technique (ps) | Novel Technique with transistor stacking (ps) | Novel technique with retention transistor (ps) |
|---|---|---|---|---|
| 0 | 102 | 122 | 212 | 123 |
| 1 | 168 | 89 | 189 | 86.69 |

Delay is minimum in novel hybrid technique with retention transistor. The simulated result of NOR gate is shown in Table VIII and IX and the output waveform is shown in figure 12.

Table VIII
DYNAMIC POWER CONSUMPTION OF NOR GATE

| INPUTS | Standard CMOS (nw) | Novel Hybrid technique (nw) | Novel Technique with transistor stacking (nw) | Novel Technique with retention transistor(nw) |
|---|---|---|---|---|
| 00 | 198.3 | 75.91 | 87.71 | 76.58 |

| | | | | |
|---|---|---|---|---|
| 01 | 48.88 | 41.85 | 36.77 | 37.39 |
| 10 | 103.5 | 26.88 | 25.97 | 22.09 |
| 11 | 188 | 60.81 | 49.29 | 62.25 |

Here novel technique with retention transistors consumes less dynamic power compared to other technique. Static power consumption is less in case of novel technique with transistor stacking and hybrid technique.

Table IX
STATIC POWER CONSUMPTION OF NOR GATE

| INPUTS | Standard CMOS (pw) | Novel Hybrid technique (pw) | Novel Technique with transistor stacking (pw) | Novel Technique with retention transistor(pw) |
|---|---|---|---|---|
| 00 | 8.289 | 2.636 | 2.595 | 46.06 |
| 01 | 3.946 | 1.88 | 2.167 | 34.37 |
| 10 | 3.686 | 0.669 | 0.653 | 0.703 |
| 11 | 1.951 | 0.6209 | 0.63 | 0.576 |

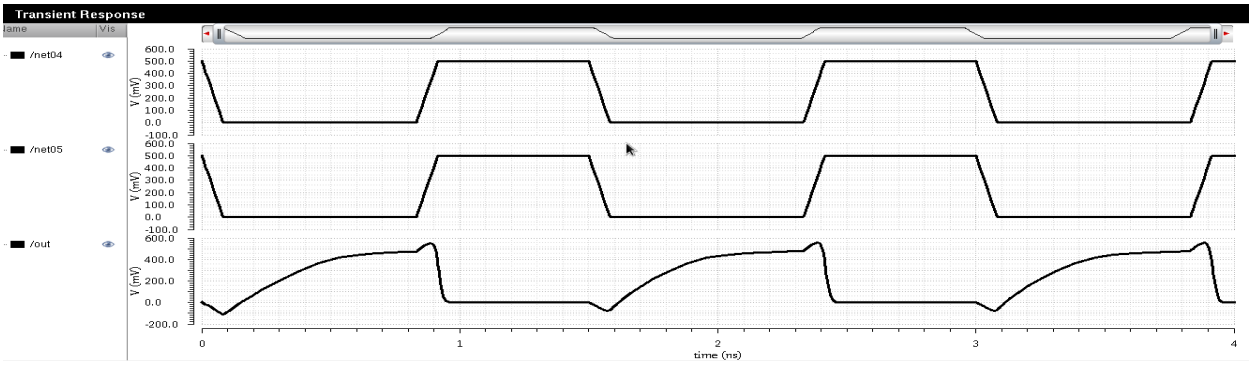

Fig 12. Novel Hybrid NOR gate with retention transistor

Table X
DELAY OF NOR GATE

| INPUT | Standard CMOS (ps) | Novel Hybrid Technique(ps) | Novel Technique with transistor stacking(ps) | Novel technique with retention transistor(ps) |
|---|---|---|---|---|
| 0 | 116.69 | 46.47 | 58.32 | 48 |
| 1 | 334 | 297.2 | 646 | 299 |

Delay is less in novel technique with retention transistors as extra transistors are added for state retention, helps in quick low to high transition and thereby the delay is minimized as shown in table X

From the ideas obtained we tried to reduce the power consumption of a full adder. For that a 10T full adder is considered. Figure 13 shows schematic of 10T full adder[15]

cell designed using CMOS 45 nm technology consist energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. It also uses the sleep transistors to reduce the leakage power. The circuit consists of two xors realized by 4 transistors. Sum is obtained from the output of the second stage xor circuit. The cout can be obtained by multiplexing a and c which is controlled by the output of a xor b. Let us consider that there is a capacitor at the output node of the first XOR module. The charge stored at the load capacitance is reapplied to the control gates. The combination of not having a direct path to ground (depends on input) and the re-application of the load charge to the control gate makes the 10T full adder an energy efficient design. The circuit produces full-swing at the output nodes. But somewhat less to provide so for the internal nodes. A

Table XI
DYNAMIC POWER CONSUMPTION OF 10T FULL ADDER

| 10T full adder circuit (nw) | 10T fulladder circuit using sleep transistor(nw) |
|---|---|
| 62.57 | 53.9 |

Table XII
STATIC POWER CONSUMPTION OF 10T FULL ADDER

| 10T full adder circuit (pw) | 10T full adder circuit using sleep transistor(pw) |
|---|---|
| 4.436 | 0.383 |

From the result it is clear that the power is reduced by four times in the proposed design.

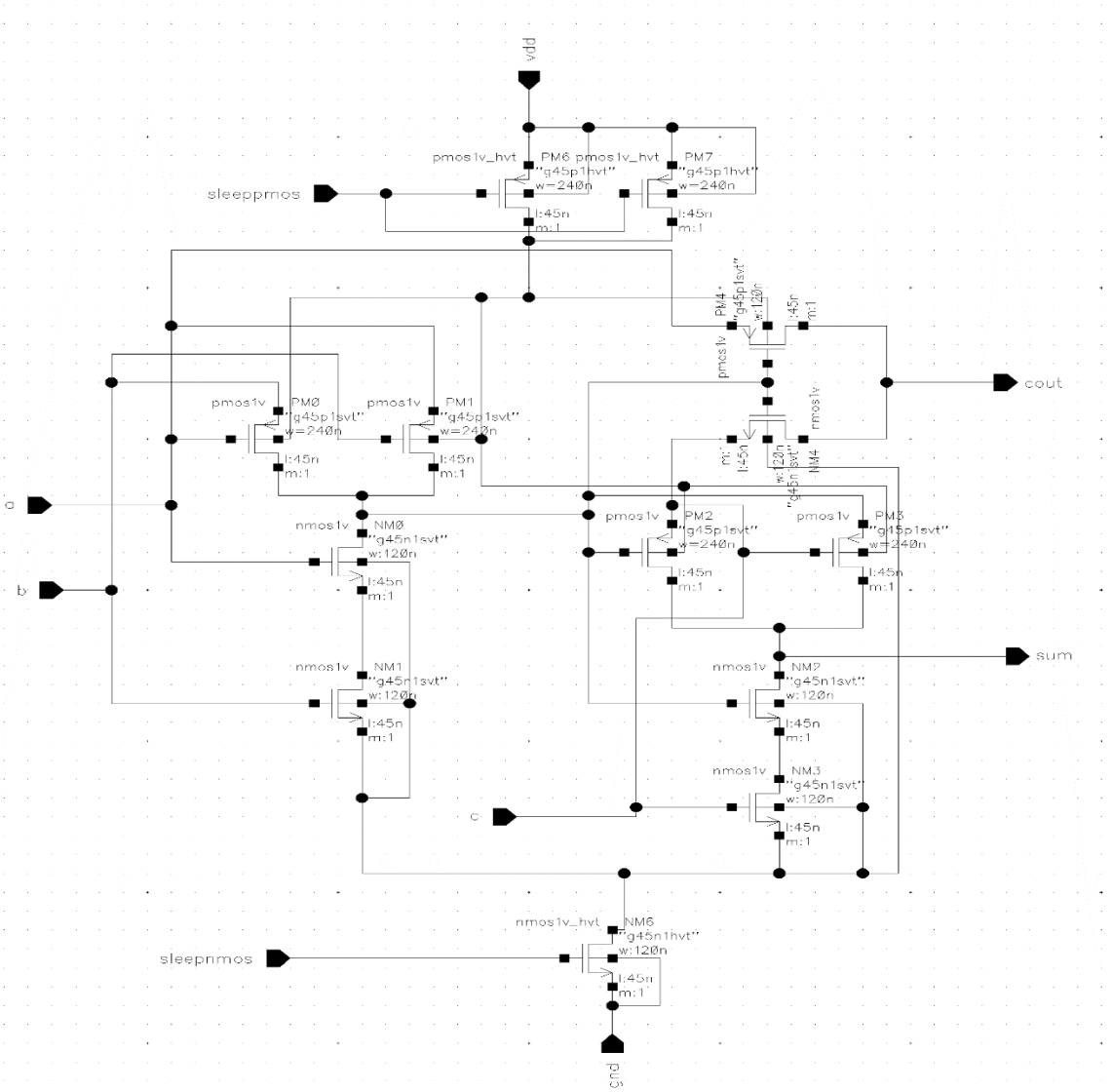


Fig 13.Schematic diagram of 10T full adder with sleep transistors

## Conclusion

We have proposed three techniques to reduce the power consumption of logic gates and the design is extended for the performance analysis of 10T full adder. Voltage scaling is one of the most efficient ways for reducing power and energy. For ultra-low voltage operation, techniques which allows bulk CMOS circuits to work in the sub-0.5V supply territory is presented. We are also reducing the leakage power with the help of power gating techniques. The hybrid multiple mode power gating reduces the static power, delay as well as power delay product.

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