Low Power Dissipation in Adder using Isolated Sleepy Keeper Approach

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Abstract- Arithmetic adder is basic of all computation or calculation so if it is improved with decreasing power so it will lead to better result. Approaches like sleepy keeper technique, sleepy keeper using isolated sleepy keeper technique are discussed to reduce power and their simulation is done on cadence low power kit to get result. There are disturbances from the input which lead to disturbance in the output, which is assumed to be stable in case of sleepy keeper approach. This disturbance creates swings and introduce noise in such a way that signal cannot be recognized any more. Isolated Keeper approach can retain the output in sleep state even in the case of disturbance. With this approach, a considerable reduced dynamic power is obtained at the cost more power in static state. Low dynamic power leads to good efficiency of device.

Index Terms- Static power, Dynamic power, Sleepy keeper approach, Isolated Sleepy keeper approach.

I. INTRODUCTION

Addition, subtract, multiply, division are some regular operations called arithmetic that are generally utilized as a part of microelectronic frameworks. Addition is a fundamental operation of any arithmetic process and is the fundamental or pillar of numerous other customarily utilized math operations. Accordingly, 1-bit Full Adder cell is the most critical and fundamental square of a number mathematical unit of a framework. Clearly, enhancing its power straightforwardly prompts enhancing the execution of the entire framework The wide utilization of this operation in math capacities, have made numerous analysts anxious to propose a few sorts of various rationale styles for actualizing 1-bit Full Adder cell. The increase in business of convenient gadgets, for example, mobile phones, gaming reassures, and so forth require microelectronic devices plan with low power dissipation. As the extent of chip, combination and multifaceted nature of the chips keep on increasing, and then heat or power is expanding then cool it down, increment the cost and usefulness of the processing frameworks. As the innovation increases to 65nm there is not as much increment in unique power dissipation but rather the static or leakage power is same or surpass when the dynamic power increment past 65nm technology. In this way the procedures used to control power is not restricted to dynamic power [1-3]. At different theoretical levels control streamlining in a processor can be accomplished. Framework or Algorithm or Architecture have a more potential for power sparing even these methods tend to expand greater usefulness on an Integrated Circuit. So improvement at Circuit and Technology level is likewise vital for scaling down of ICs. Add up to Power dissipation in a CMOS circuit is total of dynamic power, static or spillage control. Plan for low-control suggests the capacity to diminish every one of these segments of energy utilization in CMOS circuits amid the improvement of a new low power electronic item.

II. TECHNIQUES FOR LOWERING THE POWER LEAKAGE

2.1 Dynamic Power Suppression

Dynamic/Switching power happens in view of charging and discharging of load capacitors of a circuit [1-2]. Scaling of supply voltage has been the most embraced approach for power optimization, since it yields broad power speculation stores in view of the quadratic dependence of trading/dynamic power on supply voltage V_{DD}. The real disadvantage of this approach is that cutting down the supply voltage impacts circuit speed. So both design or outline and innovative or technology arrangements must be connected to repay the lessening in circuit execution exhibited by reduced voltage. A portion of the systems regularly used to lessen dynamic power are portrayed underneath.

2.2 Adiabatic Circuits

In adiabatic circuits as opposed to dissipating the power, a similar power is reused. By remotely control the shape and length of signal transition power consumed by flip a bit can be diminished or reduce to little values [2-3]. Diodes are not utilized as a part of outline of adiabatic circuit since diodes are thermodynamically irreversible. MOSFETs ought not to be turned ON and OFF when there is noteworthy potential contrast amongst source and drain when there is a huge current passing through the device separately.

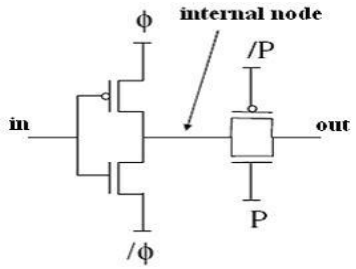

Figure 1 Charge Recovery Logic [3]

In the above adiabatic circuit at first, ø and /ø at $V_{dd/2,}$ P at Gnd, and/P at Vdd. On substantial or valid input and by step by step swinging P and/P, the pass gate is turned on. Rails ø and /ø "split", step by step or gradually swinging to V_{dd} and Gnd. When the output is examined, pass gates are off. Whenever ø and /ø bit by bit swing to $V_{dd/2}$ then the interior node is re-established or restore. Once the device is ON, the vitality move happens in a controlled way so that there is no potential drop over the gadget or a circuit.

2.3 Logic Design for Low Power

During the outline of circuit, different decisions are made, for example, Choices between static versus dynamic topologies, standard CMOS versus pass-transistor rationale styles and synchronous versus Asynchronous planning styles [3-4] . In static CMOS circuits, about the 10% of the aggregate power utilization is because of short out current. In unique circuits there is no such issue, in light of the fact that there is no any prompt dc path from supply voltage. i.e. vdd to ground. There is such a way, exit just in domino-logic circuits so as to decrease sharing; henceforth there is a less measure of short out power dissipation. We can also use the pass transistor logic to exploit reduced swing to lower power.

$$P = CL*Vdd* (Vdd-Vt) \quad (1)$$

2.4 Reducing Glitches

At the point when two parallel driving common gate at various times then Glitches happen in a logic chain. The output changes to incorrect for a short minute before settling to right outcome. Consider circuit appeared as underneath [4-5]. Give us a chance to expect at first that without buffer, path A is fast and Path B is moderate. So if A=1 and B=1 then Z=0.Next if B is to change to 0 and A to 0 since B is moderate the information 0 touching base at B will be direct and along these lines Z switches towards 1 promptly before changing back to 0 realizing power dissipation.

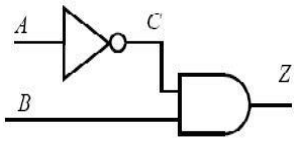

Figure 2 CMOS AND circuit [3]

2.5 Logic level power optimization

During logic optimization for low power, technology parameters, for example, supply voltage are settled or fixed and the degrees of flexibility are in choosing the usefulness and estimating the gates. Path equalization with buffer insertion is a strategy which guarantees that flag signal from inputs to output of a logic network follows ways of comparative length to overcome glitches [3-5]. So when ways are leveled or equalized a large portion of the gates have adjusted moves at their information sources, which limiting the exchanging action or glitches. Another logic level power minimization systems which incorporate neighborhood changes is appeared in figure beneath .In this re-mapping change a high-movement node which is set apart with set apart with x is evacuated and supplanted by new mapping.

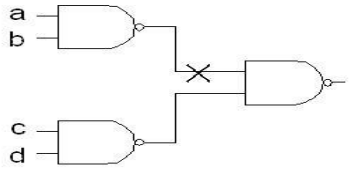

Figure 3 Logic Remapping for Low Power [3]

2.6 Standby Mode Leakage Suppression

Substrate current and sub threshold leakage produces the static and leakage control. For technology of 1 µm or more from 1um, switching force was dominating. Yet, for deep submicron forms underneath 180nm, Leakage control ends up predominant element [6]. Since Leakage control impacts battery lifetime subsequently it is a noteworthy worry in later technology. At the point when transistors are either not exchanging or in remain by mode then CMOS technology has been to a great degree control effective , and is normal by the framework designer ,the low leakage from CMOS chips. To meet our necessities identified with leakage control constraints, numerous edge and variable limit circuit procedures are utilized [5-6]. In various edge CMOS, the procedure gives two different sort of limit transistors.

(1) Low-edge transistors are utilized on speed fundamental sub-circuits and they are fast.
(2) High-edge transistors are slower yet make low sub-edge spillage, and they are used as a piece of noncritical or direct methods for the chip.

As more transistors progress toward becoming planning basic then various limit strategies prompts lose adequacy or effectiveness.

2.7 Variable Body Biasing

Variable body biasing circuits control the limit voltage of transistors utilizing substrate biasing and in this manner deficiency related is overcome with multi threshold design or outline [8-10]. At the point when a variable-limit of circuit is in standby mode, then NMOS transistors substrate is negative biased, and the threshold increments because of the body bias impact. In this manner similarly, PMOS transistors substrate is positive body bias to expand their V tie the threshold in standby mode in a principal, Variable threshold circuits can, take care of the static leakage issue, yet they require controlling circuits that regulate substrate voltage in standby mode. Quick and accurate body bias control with control circuit is a major challenge and it requires carefully designed closed-loop control. At the state when the circuit is idle mode, the bulk or body of both PMOS and NMOS are biased by supply voltage to build the limit voltage, V_t of the MOSFET. However, in typical operation they are changed back to lessen the V_t.

2.8 Dynamic Threshold MOS

In dynamic threshold CMOS i.e. DTMOS, the limit voltage is changed to suit the working condition of the circuit. A high threshold voltage in the standby mode gives the low leakage current, while a low limit voltage in the dynamic mode takes into account higher current drives [7-8]. Dynamic threshold CMOS can be obtained by tying the gate alongside the body. The diode build in potential in mass silicon technology is utilized to restrict the supply voltage of DTMOS. The PN diode amongst source and body ought to be turn reversed biased. Hence, this method is reasonable for ultralow voltage circuits in mass CMOS going from 0.6V and underneath.

2.9 Short Circuit Power Suppression

At the point when sets of PMOS/NMOS transistors are directing at the same time it cause the short circuit current which prompts to short circuit power [8-10]. The short out way exists for direct current spill out of v_{dd} to gnd. One approach to diminish short circuit power is to keep the fall time and rise time same. On the off chance that $V_{dd} < V_{tn} + |V_{tp}|$ then short out power can be dispensed with.

III. TECHNIQUES FOR THE SIMULATION

3.1 Sleepy keeper approach

In sleepy keeper approach, a NMOS transistor having high threshold value limit is associated in parallel with the PMOS transistor to which sleep signal is given and a PMOS transistors having high threshold value limit is associated in parallel with the NMOS to which sleep bar signal is given are associated in a pull down network [6-8].The current situation with the circuit can be held in rest mode and furthermore decreases sub edge leakage control essentially .Result of this paper is that the tired attendant is the best way to deal with limit the static power in computerized VLSI circuit.

3.2 Isolated Sleepy Keeper Approach

This approach includes the techniques as we discussed previously except one that is isolated sleepy keeper technique [6-8]. It states that the sleepy keeper approach is good in getting the output in sleep state but if there is any disturbance in sleep state from input then there will be voltage swing at output therefore to isolate the output from the network in such a way that no disturbance should be transferred from base network or from input to the output during the sleep mode, isolated sleepy keeper approach is introduced. The pass transistor can pass only 1or 0. Therefore instead of pass transistor, transmission gate is used which can pass both 1 and 0 in an efficient manner in active modes is 'set' to 0 and 'not s' is set to 1 then whatever will be result it pass to the output .in sleep mode's' is set to 1 and 'not s' is set to 0 then both transistors of transmission gate are off and output is isolated from the base network.

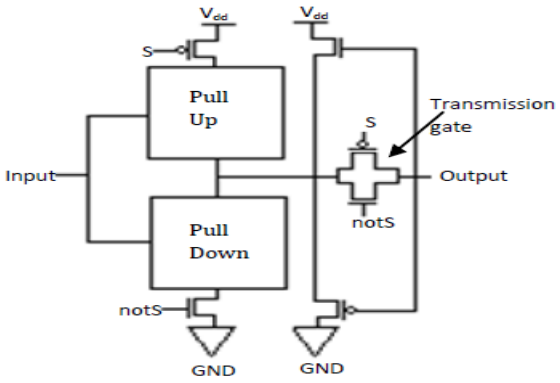

Figure 4 Isolated sleepy keeper network [6]

IV. RESULTS

All the designs are simulated in the spectre circuit simulator in cadence. It creates the netlist for DC, AC or transient analysis. Low power unit empowers groups with restricted involvement in actualizing propelled low-control procedures which help the group to embrace them in their outline with essentially hazard is decreased. It enhances the efficiency noteworthy through provided framework. Through the use of demonstrated procedures the timetable consistency re-establishes or re construct. It helps in keeps away from normal issues in low-control plan through practices and master learning. Low control kit advances flows and trade off to guarantee that the utilized technology is giving best outcome or not which may prompt enhance nature of silicon. It also reduces overall packaging and system cost.

Sleep keeper approach and isolated sleep keeper approach have been applied to inverter and full adder to analyze the reduced power. Tabular comparative analysis is also done for the considered low power techniques with base design and sleepy keeper approach .So inverter and full adder circuits with their results are considered in this section.

4.1 Inverter

Inverter is used to invert the input. It is basically a 'NOT' gate

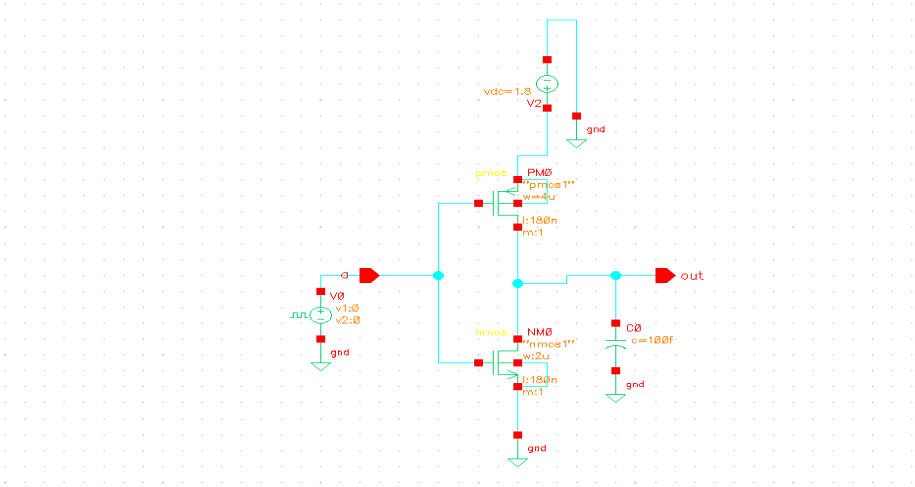

Figure 5 Circuit diagram of inverter

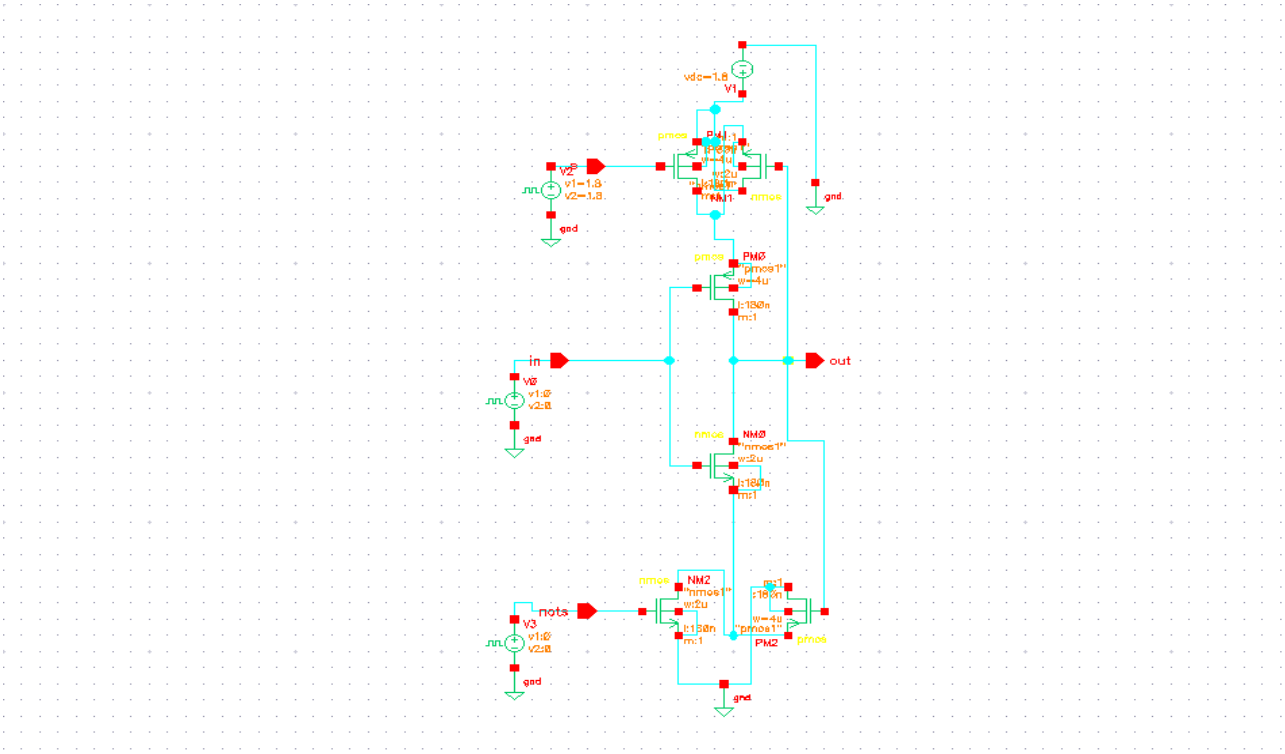

Figure 6 Circuit diagram of inverter using sleepy keeper approach

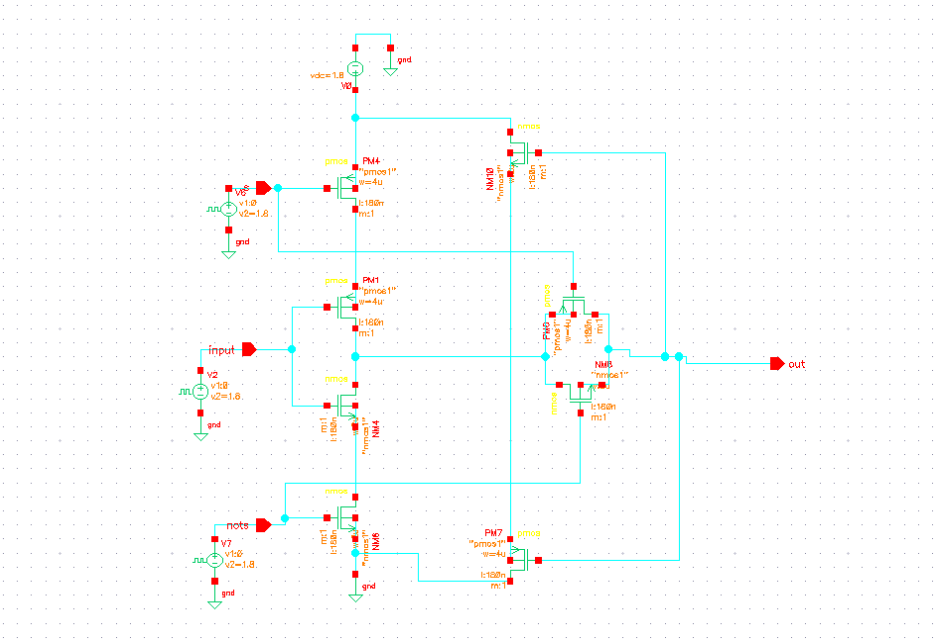

Figure 7 Circuit diagram of an Inverter using isolated sleepy keeper approach

Table 1 Comparison of power of an inverter with different approach

NETWORKS	TOTAL POWER	STATIC POWER	DYNAMIC POWER
BASE INVERTER	7.53E-06	2.73E-11	7.52E-06
INVERTER WITH SLEEPY KEEPER APPROACH	1.0E-6	1.41E-11	1.00E-06
INVERTER WITH ISOLATED SLEEPY KEEPER APPROACH	7.46E-07	2.04E-11	7.47E-07

From table 1, it is clear that isolated sleepy keeper approach is much effective for the total power dissipation in the simulated inverter. In the static power, the change is not significant, but for the dynamic power a significant change has been observed.

4.2 Full Adder

Full adder adds the binary numbers .For example the for one bit full adder it has three input say a, b, cin and it provide output sum and carry .

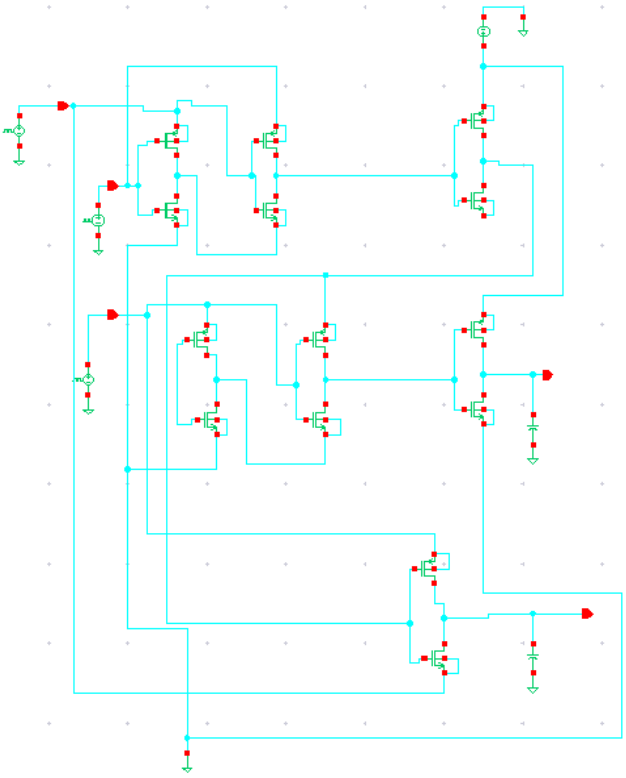

Figure 8 Circuit diagram of full adder

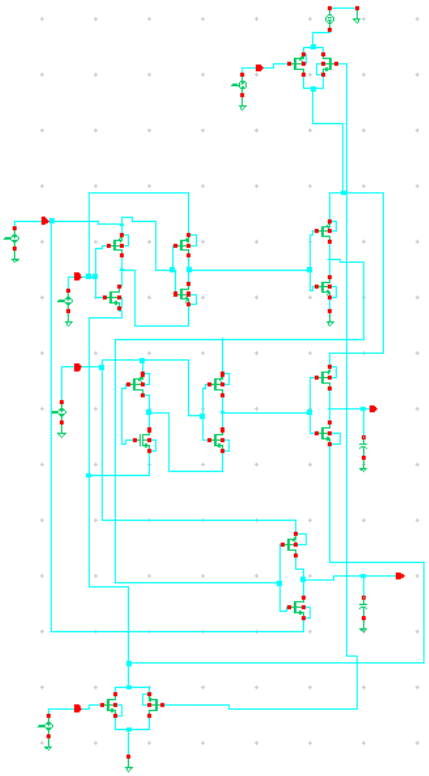

Figure 9 Circuit diagram of full adder using sleepy keeper approach

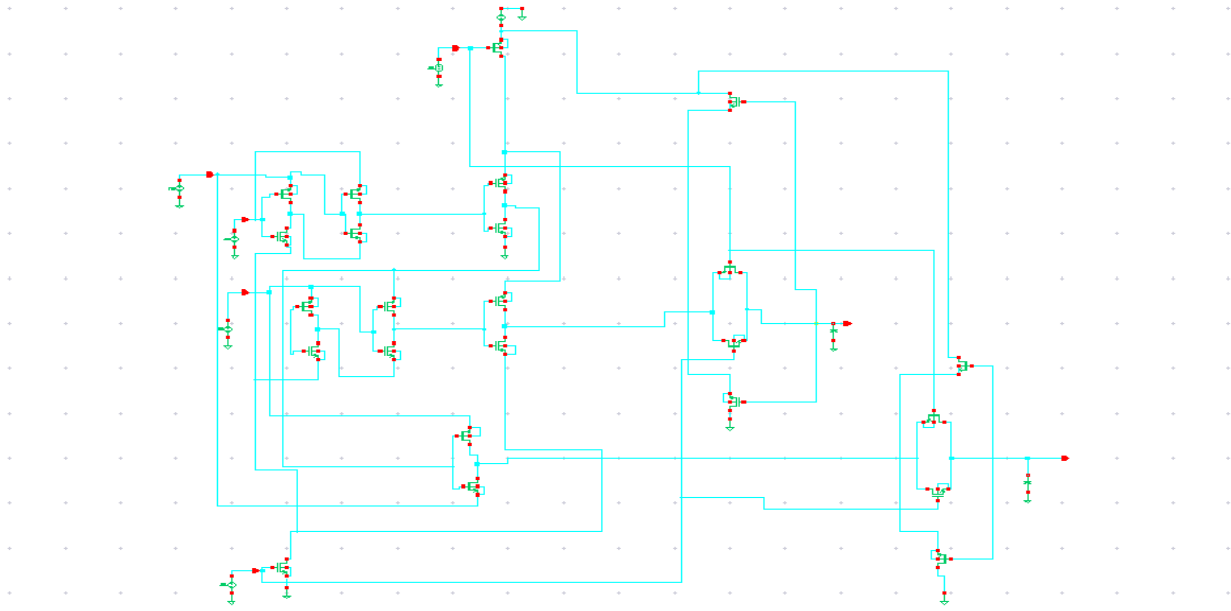

Figure 10 Circuit diagram of full adder using isolated sleepy keeper approach

Table 2 Comparison of power of full adder with different approaches

NETWORK	TOTAL POWER	STATIC POWER	DYNAMIC POWER
FULL ADDER	2.07E-07	7.12E-11	2.07E-07
FULL ADDER WITH SLEEPY KEEPER APPROACH	5.92E-07	9.32E-12	5.92E-07
FULL ADDER WITH ISOLATED SLEEPY KEEPER APPROACH	5.71E-08	1.86E-11	5.71E-08

From table 2, it is clear that isolated sleepy keeper approach is much effective for the total power dissipation in the simulated full adder. In the static power, the change is not significant, but for the dynamic power a significant change has been observed.

V. CONCLUSION

Approaches like sleepy keeper technique, isolated sleepy keeper technique are discussed to reduce power and their simulation is done on cadence low power kit to get results. These approaches are implemented on circuits of Inverter and Full Adder. With the approach of isolated sleepy keeper technique, a significant improvement has been observed in the power dissipation. Adders are the integral part for high speed multipliers and for other arithmetic operations and a significant power reduction in one cell can contributes to high power reduction in the complete digital integrated circuits. This research work further can be expanded to apply this approach on memory designs and advanced high speed adders.

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